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SRI VASAVI ENGINEERING COLLEGE (AUTONOMOUS)

(Sponsored by Sri Vasavi Educational Society)
Approved by AICTE, New Delhi and Permanently Affiliated to JNTUK, Kakinada
Pedatadepalli, **TADEPALLIGUDEM – 534 101,** W.G. Dist, (A.P.)

Department of Electronics and Communication Engineering

Dt: 28-12-2020

Fourth meeting of BOS in ECE department along with external members was held on 28/12/2020 at 2.00 PM in online mode through Zoom meeting app with the link https://us02web.zoom.us/j/83813811675 in view of COVID-19 pandemic.

The following members are present.

S. No	Name of the BOS Members
1.	Dr. I. Shanthi Prabha, Prof, JNTUK,Kakinada
2.	Prof. NVSN. Sarma, Director, IIIT, Trichy
3.	Dr. M. Venugopala Rao, Professor, KL University, Vijayawada
4.	Sri S.Siva Kumar, Senior Engineer, Qualcomm, Bangalore.
5.	Dr. GVNSR. Ratnakar Rao, Principal, Sri Vasavi Engineering College
6.	Dr. E. Kusuma Kumari, Chairman & HOD, SVEC
7.	All the Internal BOS members

Minutes of 4th BOS Meeting

Item No 1: **Welcome Note by the Chairperson BOS**.

The Chairperson welcomed all the BOS members and introduced to all the BOS-internal members.

Item No.2: Review and approval of course structure of I & II semesters of B. Tech (ECE & ECT) under V20 Regulations.

Reviewed the Course structure of I & II Semesters for UG (B. Tech – ECE & ECT) Programme of V 20 Regulation and the approved course structure is attached in **Annexure-I.**

Item No.3: Approval of syllabi for the courses offered by the department in I & II semesters B. Tech under V20 Regulation.

Members Suggested that for the course Switching Theory and Logic Design(V20ECT01), identify is there any relevant course in NPTEL and if so follow the course outcomes given in NPTEL Course.

The NPTEL Course Titled Digital Circuits is relevant to Course "Switching Theory and Logic Design" (V20ECT01) and course outcomes are modified accordingly.

Members Approved the syllabi for the courses by the department in I & II semesters B. Tech under V20 Regulation and details are attached in **Annexure-II.**

E. Kumaraswamy

CHAIRPERSON OF BOS

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Department of Electronics and Communication Engineering

COURSE STRUCURE FOR FIRST YEAR B.TECH ECE & ECT

(FOR 2020-21 ADMITTED BATCH) I Semester

Sl. No	Category	Course Code	Course Title	Hours per week			Credits
				L	T	P	C
1	Basic Science Course		M-I	3	0	0	3
2	Basic Science Course		Engg. Physics	3	0	0	3
3	Humanities and Social Science Course		English	3	0	0	3
4	Engg. Science Courses		Basic Electrical Engineering	3	0	0	3
5	Engg. Science Courses		Engg. Graphics	1	0	4	3
6	Humanities and Social Science Lab		English Lab- 1	0	0	3	1.5
7	Basic Science Course Lab		Engg. Physics Lab	0	0	3	1.5
8	Engg. Science Course Lab		Basic Electrical Engineering Lab	0	0	3	1.5
	Mandatory Course (AICTE Suggested)		Environmental Science	3	0	0	0 (MNC)
						Total Credits	**19.5**

II Semester

Sl.No	Category	Course Code	Course Title	Hours per week			Credits
				L	T	P	C
1	Basic Science Course		M-II	3	0	0	3
2	Basic Science Course		Chemistry	3	0	0	3
3	Engg. Science Courses		Programing “C” for Problem Solving	3	0	0	3
4	Engg. Science Courses		Engg. Workshop	3	0	0	3
5	Engg.Science Courses	V20ECT01	Switching Theory & Logic Design	3	0	0	3
6	Engg. Science Course Lab		Programing “C” for Problem Solving Lab	0	0	3	1.5
7	Basic Science Course Lab		Chemistry Lab	0	0	3	1.5
8	Humanities and Social Science Lab		English Lab-II	0	0	3	1.5
						Total Credits	**19.5**

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Department of Electronics and Communication Engineering

Switching Theory and Logic Design
Syllabus

Academic Year: 2020-2021
Year/ Semester: II semester
Programme: B.Tech
Section: ECE A, B ,C& ECT

Name of the Course: STLD
Course Code: **V20ECT01**

Course Outcomes (CO's) (Along with Knowledge Level (K)):

After going through this course the student will be able to

CO_x	K_x	Course Outcome
CO-1	K_2	**Explain** the different types of number Systems, number conversions, codes and logic Gates.
CO-2	K_3	**Apply** the concepts of Boolean algebra and use the knowledge of K-maps and tabular method for minimization of Boolean expressions.
CO -3	K_3	**Construct** the higher order modules from their lower order structures of various combinational logic circuits.
CO-4	K_2	**Explain** the concept of various flip flops
CO-5	K_3	**Develop** various sequential circuits like registers, counters by using basic flip flops.
CO-6	K_3	**Develop** the various Finite State Machine Models

Unit – I: **Number Systems & Codes:**

i) Representation of numbers of different radix, conversation from one radix to another radix, r-1's compliments and r's compliments of signed members, problem solving. ii) 4 bit codes, BCD, Excess-3, 2421, 84-2-1 9's compliment code etc., iii) Logic operations and error detection & correction codes; Basic logic operations -NOT, OR, AND, Universal building blocks, EX-OR, EX-NOR -Gates, Gray code, error detection, error correction codes (parity checking, even parity, odd parity, Hamming code).

Unit – II : **Minimization Techniques**

Boolean theorems, principle of complementation & duality, De-morgan theorems, minimization of logic functions using Boolean theorems, Standard SOP and POS, Forms, NAND-NAND and NOR-NOR realizations, minimization of switching functions using K-Map up to 5 variables, tabular minimization, problem solving (code-converters using K-Map etc..).

Unit – III : **Combinational Logic Circuits Design**

Design of Half adder, full adder, half subtractor, full subtractor, applications of full adders, 4-bit binary subtractor, adder-subtractor circuit, BCD adder circuit, Excess 3 adder circuit, look-a-head adder circuit, Design of decoder, demultiplexer, 7 segment decoder, higher order demultiplexing, encoder, multiplexer, higher order multiplexing, realization of Boolean functions using decoders and multiplexers, priority encoder, 4-bit digital comparator.

Unit – IV : **Sequential Circuits –I**

Classification of sequential circuits (synchronous and asynchronous); basic flip-flops, truth tables and excitation tables (Nand RS latch, nor RS latch, RS flip-flop, JK flip-flop, T flip-flop, D flip-flop with reset and clear terminals). Asynchronous Inputs (Preset and Clear), Race around condition, Master Slave JK Flip flop, Conversion from one flip-flop to another flip-flop.

Unit – V : **Sequential Circuits -II**

Design of ripple counters, design of synchronous counters, Johnson counter, ring counter. Design of registers - Buffer register, control buffer register, shift register, bi-directional shift register, universal shift register.

Unit – VI : **Finite State Machines**

Finite State machine; Analysis of Clocked sequential circuits, state Diagrams, state Tables, Reduction of State Tables and State assignments, design Procedures. Realization of Circuits using various Flip Flops. Meelay to Moore Conversion and Vice-versa.

Text Books

1. Digital Design by M. Morris Mano, Michael D. Ciletti, PEA.
2. Switching & Finite Automata Theory, 2nd Edition, Zvi Kohavi, TMH,1978
3. Fundamentals of Logic Design, 5/e Roth, Cengage.

Reference Books

1. Modern Digital Electronics by RP Jain, TMH
2. An Engineering Approach to Digital Design, William I. Fletcher, Pearson edition.
3. Switching Theory and Logic Design by A. Anand Kumar

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Department of Electronics and Communication Engineering

Switching Theory and Logic Design

Syllabus

Academic Year: 2020-2021 **Programme:** B.Tech
Year/ Semester: II semester **Section: ECE** A, B ,C& ECT

Name of the Course: STLD **Course Code:** **V20ECT01**

Course Outcomes (CO's) (Along with Knowledge Level (K)):

After going through this course the student will be able to

CO_x	K_x	Course Outcome
CO-1	K_2	**Explain** the different types of number Systems, number conversions, codes and logic Gates.
CO-2	K_3	**Apply** the concepts of Boolean algebra and use the knowledge of K-maps and tabular method for minimization of Boolean expressions.
CO -3	K_3	**Construct** the higher order modules from their lower order structures of various combinational logic circuits.
CO-4	K_2	**Explain** the concept of various flip flops
CO-5	K_3	**Develop** various sequential circuits like registers, counters by using basic flip flops.
CO-6	K_3	**Develop** the various Finite State Machine Models

Unit – I: **Number Systems & Codes:**

i) Representation of numbers of different radix, conversation from one radix to another radix, r-1's compliments and r's compliments of signed members, problem solving. ii) 4 bit codes, BCD, Excess-3, 2421, 84-2-1 9's compliment code etc., iii) Logic operations and error detection & correction codes; Basic logic operations -NOT, OR, AND, Universal building blocks, EX-OR, EX-NOR - Gates, Gray code, error detection, error correction codes (parity checking, even parity, odd parity, Hamming code).

Unit – II : **Minimization Techniques**

Boolean theorems, principle of complementation & duality, De-morgan theorems, minimization of logic functions using Boolean theorems, Standard SOP and POS, Forms, NAND-NAND and NOR-NOR realizations, minimization of switching functions using K-Map up to 5 variables, tabular minimization, problem solving (code-converters using K-Map etc..).

Unit – III : **Combinational Logic Circuits Design**

Design of Half adder, full adder, half subtractor, full subtractor, applications of full adders, 4-bit binary subtractor, adder-subtractor circuit, BCD adder circuit, Excess 3 adder circuit, look-a-head adder circuit, Design of decoder, demultiplexer, 7 segment decoder, higher order demultiplexing, encoder, multiplexer, higher order multiplexing, realization of Boolean functions using decoders and multiplexers, priority encoder, 4-bit digital comparator.

Unit – IV : **Sequential Circuits –I**

Classification of sequential circuits (synchronous and asynchronous); basic flip-flops, truth tables and excitation tables (Nand RS latch, nor RS latch, RS flip-flop, JK flip-flop, T flip-flop, D flip-flop with reset and clear terminals). Asynchronous Inputs (Preset and Clear), Race around condition, Master Slave JK Flip flop, Conversion from one flip-flop to another flip-flop.

Unit – V : **Sequential Circuits -II**

Design of ripple counters, design of synchronous counters, Johnson counter, ring counter. Design of registers - Buffer register, control buffer register, shift register, bi-directional shift register, universal shift register.

Unit – VI : **Finite State Machines**

Finite State machine; Analysis of Clocked sequential circuits, state Diagrams, state Tables, Reduction of State Tables and State assignments, design Procedures. Realization of Circuits using various Flip Flops. Meelay to Moore Conversion and Vice-versa.

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4. Digital Design by M. Morris Mano, Michael D. Ciletti, PEA.
5. Switching & Finite Automata Theory, 2nd Edition, Zvi Kohavi, TMH
6. Fundamentals of Logic Design, 5/e Roth, Cengage.

Reference Books

4. Modern Digital Electronics by RP Jain, TMH
5. An Engineering Approach to Digital Design, William I. Fletcher, Pearson edition.
6. Switching Theory and Logic Design by A. Anand Kumar

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Department of Electronics and Communication Engineering

Digital Logic Design

(To II Sem CSE& CST Students Offered by ECE Dept)

Academic Year: 2020-2021
Year/ Semester: II semester

Programme: B.Tech
Section: CSE -A, B , C, D & CST

Name of the Course: DLD

Course Code: V20ECT02

Course Outcomes (CO's) (Along with Knowledge Level (K)):

After going through this course the student will be able to

CO_x	K_x	Course Outcome
CO-1	K_3	Illustrate the conversion of a number from one number system to another
CO-2	K_2	Classify Boolean theorems & simplify the Boolean functions using the Boolean properties
CO-3	K_3	Use K-map as a tool to simplify and design logic circuits
CO-4	K_3	Construct different combinational Logic circuits like MUX, Decoders, Encoders etc
CO-5	K_3	Demonstrate the basic flip-flops in terms of truth table & excitation table
CO-6	K_3	Apply the concepts of flip-flops in the designing of different sequential circuits like registers, counters, etc

SYLLABUS:

UNIT-I: Number systems& Binary codes:

Review of Number systems: Decimal, Binary, Octal, Hexadecimal number systems, Conversation from one radix to another radix, r's and (r-1)'s complement of signed numbers.

Binary codes: 8421, 2421, 84-2-1, BCD code, Gray code, Excess-3 codes.

UNIT -II: Concept of Boolean algebra:

Boolean theorems, Principle of complementation & Duality, De-Morgan theorems, Minimization of logic functions using Boolean theorems**,** Canonical and Standard forms of SOP and POS.

Basic logic operations -NOT, OR, AND, Universal building blocks, EX-OR, EX-NOR and Inverted Gate

UNIT- III: Gate level Minimization:

Map Method, Two-Variable K-Map, Three-Variable K-Map, Four Variable K-Maps. Product of Sum Simplification, Sum of Products Simplification, Don't– Care Conditions, NAND and NOR realizations.

UNIT- IV: Combinational Logic Circuits:

Introduction, Analysis Procedure, Design Procedure, Half adder, Full adder, Half subtractor, Full subtractor, 4bit Binary adder–subtractor, Decimal adder, BCD adder, Decoders, Encoders, Priority Encoder, Multiplexers and De- Multiplexers.

UNIT V: **Sequential Logic Circuits**:

Classification of sequential circuits (synchronous and asynchronous)

Latches: SR Latch, D Latch, Gated SR Latch, Types of triggering

Flip flops: Basic Flip flop circuit, Truth table and Excitation tables of RS, D, JK and T Flip-flops, Asynchronous Inputs (Preset and Clear), Race around condition, Master Slave JK Flip flop, Conversion of one type of Flip flop to another

UNIT -VI: Registers and Counters:

Design of Registers - Buffer register, Controlled buffer register, Shift Register, Bidirectional shift register, Universal shift register, Applications of registers.

Design of counters - Asynchronous up/down counter, Synchronous up/down counter, Mod-N Counter, Ring counter, Johnson counter.

TEXT BOOKS:

1. Digital Design, 5/e, M.Morris Mano, Michael D Ciletti, PEA.

2. Fundamentals of Logic Design, 5/e, Roth, Cengage.

REFERENCE BOOKS:

1. Digital Logic and Computer Design, M. Morris Mano, PEA.

2. Digital Logic Design, Leach, Malvino, Saha, TMH.

3. Modern Digital Electronics, R.P. Jain, TMH